Claims

What is claimed is

1. A graphics controller circuit for upscaling a source video image to generate an upscaled video image, the source video image comprising a plurality of scan lines with each scan line comprising a set of pixel data, the graphics controller circuit comprising

an encoder circuit for receiving a set of pixel data for a first scan line of the source video image and generating a compressed data set corresponding to the set of pixel data for the first scan line;

a local memory coupled to receive and store the compressed data set;

a decoder circuit for retrieving the compressed data set in the local memory and for decompressing the compressed data set to generate a decompressed pixel data set; and

an interpolator for receiving the decompressed pixel data set and a set of pixel data for a second scan line of the source video, the interpolator interpolating the decompressed pixel data set and the set of pixel data for the second scan line to generate a set of additional pixel data comprised in the upscaled video image.

2. The graphics controller circuit of claim 1 wherein a display memory is provided for storing the set of pixel

data for the first scan line and the set of pixel data for the second scan line prior to being received by the encoding circuit and the interpolator respectively.

3. The graphics controller circuit of claim 1 wherein the decoder circuit comprises a DPCM decoder and the encoder circuit comprises a DPCM encoder.

4. The graphics controller circuit of claim 3 wherein the DPCM decoder compresses the set of pixel data for the first scan line such that resulting compressed data set comprises half the number bits compared to the number of bits in the set of pixel data for the first scan line.

5. The graphics controller circuit of claim 3 wherein the interpolator comprises a polyphase interpolator.

6. The graphics controller circuit of claim 3 wherein the DPCM encoder comprises

a first adder for receiving pixel data and a predicted value, the first adder generating a difference of the pixel data and the predicted value;

a quantizer for generating the compressed data set by quantizing the difference;

a recoverer circuit for generating a recoverer value

from the compressed data set;

a second adder for adding the recoverer value with the predicted value to generate an output; and

a predictor for generating the predicted value as a function of the output of the second adder.

7. The graphics controller circuit of claim 6 wherein the predictor comprises a set of flip-flops each for storing a bit of the output of the second adder.

8. The graphics controller circuit of claim 6 further comprising a override circuit to avoid a overload condition in DPCM decoding and encoding.

9. The graphics controller circuit of claim 8 wherein the override circuit avoids the overload condition by changing a predicted value to correspond to a present pixel data value.

10. The graphics controller circuit of claim 8 further comprising a MVA block wherein the MVA block comprises the DPCM encoder, the DPCM decoder, the override circuit and the local memory.

11. The graphics controller circuit of claim 10

further comprising

a video controller for sending a set of graphics pixels; and

a multiplexor for receiving the graphics pixels and pixel data of the upscaled video image, and for selectively sending to a display unit one of the graphics pixels and pixel data of the upscaled video image.

12. The graphics controller circuit of claim 11 wherein the encoder circuit receives pixel data of the first scan line from a display memory.

13. A computer system for displaying a source video image on a display unit, said source video image comprising a plurality of scan lines with each scan line comprising a set of pixel data, said computer system comprising

a display memory for storing graphics/text data;

a display unit; and

a graphics controller circuit receiving pixel data of said source video image and said graphics/text data, and upscaling said source video image to generate an upscaled video image prior to displaying said graphics/text and said upscaled source video image on said display unit, said graphics controller circuit comprising:

an encoder circuit for receiving a set of pixel

data for a first scan line of the source video image and generating a compressed data set corresponding to the set of pixel data for the first scan line;

a local memory coupled to receive and store the compressed data set;

a decoder circuit for retrieving the compressed data set in the local memory and for decompressing the compressed data set to generate a decompressed pixel data set; and

an interpolator for receiving the decompressed pixel data set and a set of pixel data for a second scan line of the source video, the interpolator interpolating the decompressed pixel data set and the set of pixel data for the second scan line to generate a set of additional pixel data comprised in the upscaled video image.

14. The computer system of claim 13 wherein the display memory stores the set of pixel data for the first scan line and the set of pixel data for the second scan line.

15. The computer system of claim 13 wherein the decoder circuit comprises a DPCM decoder and the encoder circuit comprises a DPCM encoder.

16. The computer system of claim 15 wherein the DPCM decoder compresses the set of pixel data for the first scan line such that resulting compressed data set comprises half the number bits compared to the number of bits in the set of pixel data for the first scan line.

17. The computer system of claim 15 wherein the interpolator comprises a polyphase interpolator.

18. The computer system of claim 15 wherein the DPCM encoder comprises:

a first adder for receiving pixel data and a predicted value, the first adder generating a difference of the pixel data and the predicted value;

a quantizer for generating the compressed data set by quantizing the difference;

a recoverer circuit for generating a recoverer value from the compressed data set;

a second adder for adding the recoverer value with the predicted value to generate an output; and

a predictor for generating the predicted value as a function of the output of the second adder.

19. The computer system of claim 18 wherein the predictor comprises a set of flip-flops each for storing a

bit of the output of the second adder.

20. The computer system of claim 18 further comprising a override circuit to avoid a overload condition in DPCM decoding and encoding.

21. The computer system of claim 20 wherein the override circuit avoids the overload condition by changing a predicted value to correspond to a present pixel data value.

22. The computer system of claim 20 further comprising an MVA block wherein the MVA block comprises the DPCM encoder, the DPCM decoder, the override circuit and the local memory.

23. The computer system of claim 22 further comprising

a video controller for sending a set of graphics pixels; and

a multiplexor for receiving the graphics pixels and pixel data of the upscaled video image, and for selectively sending to a display unit one of the graphics pixels and pixel data of the upscaled video image.

24. A method of upscaling a source video image in a graphics controller circuit, said source video image

comprising a plurality of scan lines with each scan line comprising a set of pixel data, said method comprising the steps of

receiving a first scan line of said source video image;

compressing the pixel data corresponding to said first scan line to generate a compressed data;

storing said compressed data in a local memory;

retrieving a second scan line of said source video image;

retrieving said compressed data from said memory circuit;

decompressing said compressed data to generate said pixel data;

generating a set of additional pixels by interpolating pixels in said first scan line and said second scan line wherein said additional pixels are comprised in an upscaled image of said source video image.

25. The method of claim 24 wherein said step of compressing comprises the step of using differential pulse code modulating (DPCM).

26. The method of claim 25 further comprising the steps storing said source video image in a display memory wherein said step of receiving receives said first scan line

from said display memory.

27. The method of claim wherein said step of using DPCM generates said compressed data comprising one half the number of bits compared to number of bits in the pixel data of said first scan line in the source video image.

28. A graphics controller circuit for displaying a source video image on a display unit, said source video image comprising a plurality of scan lines with each scan line comprising a set of pixel data, said graphics controller circuit comprising

a DPCM encoder circuit for receiving a set of pixel data for a first scan line of said source video image and generating a compressed data set using DPCM encoding scheme corresponding to the set of pixel data of the first scan line;

a local memory coupled to receive and store the compressed data set;

a DPCM decoder circuit for retrieving said compressed data set in said local memory and for decompressing said compressed data set to generate a decompressed pixel data set;

an interpolator for receiving said decompressed pixel data set and a set of pixel data for a second scan line of

said source video, said interpolator interpolating the decompressed pixel data set and the set of pixel data for the second scan line to generate a set of additional pixel data comprised in the upscaled image;

a video controller for receiving a graphics/text data from a host, and generating a corresponding pixel data; and

a multiplexor for selectively forwarding to said display unit either pixel data corresponding to said graphics/text data or pixel data of said upscaled image.